GSV6502

1 In to 2 Out HDMI 2.1 Splitter with Embedded MCU

April, 2022

Preliminary Product Specification

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Glossary

DDC	Display Data Channel
EDID	Extended Display Identification Data
ESD	Electrostatic Discharge
HDCP	High-bandwidth Digital Content Protection
HDMI	High-Definition Multimedia Interface
HPD	Hot Plug Detect
I^2C	Inter-Integrated Circuit
MCU	Microcontroller Unit
MISO	Master In Slave Out
MOSI	Master Out Slave In
OTP	One Time Programmable
PCM	Pulse Code Modulation
S/PDIF	Sony/Philips Digital Interface Format
SPI	Serial Peripheral Interface
TMDS	Transition Minimized Differential Signaling
SCDC	Status and Control Data Channel
CEC	Consumer Electronics Control
DDC/CI	VESA Display Data Channel/Command Interface
MCCS	Monitor Control Command Set (VESA)
DSC	Display Stream Compression
FEC	Forward Error Correction
HBR	HDMI High Bit-Rate Audio
SSC	Spread-Spectrum Clock

1. General Description

1.1 General Information

Gscoolink GSV6502 is a high-performance, low-power 1 In to 2 Out HDMI 2.1 to HDMI 2.1 splitter. By integrating enhanced microcontroller based on RISC-V, GSV6502 has created a cost-effective solution that provides time-to-market advantages. GSV6502's HDMI Receiver and HDMI Transmitter supports up to 48Gbps (FRL, 12G/4Lane). The superior architecture of GSV6502 provides economical smaller footprint solutions using QFN88, targeting applications of Consumer and ProAV.

GSV6502 supports all uncompressed HDMI input video/audio decoding/encoding and DSC stream pass-through to HDMI output. HDCP 1.4 and HDCP 2.2/2.3 are implemented in GSV6502 for both HDMI Input and Output in HDMI 2.0 and FRL mode. HDR-SDR Conversion, Deinterlacer, Downscaler, 444-420 Conversion, Color Space Conversion are supported in HDMI Tx in HDMI 2.0 and FRL mode. Flexible implementations of Audio Insertion, Audio Extraction and SPDIF to I2S conversion are supported in GSV6502. Embedded CEC engine enables flexible remote control of the entire HDMI signal chain.

An internal Video Generator can be used to generate any uncompressed video timing defined in HDMI 2.1, such as 8K@60Hz, 8K@30Hz, 4K@120Hz, 480i@60Hz.

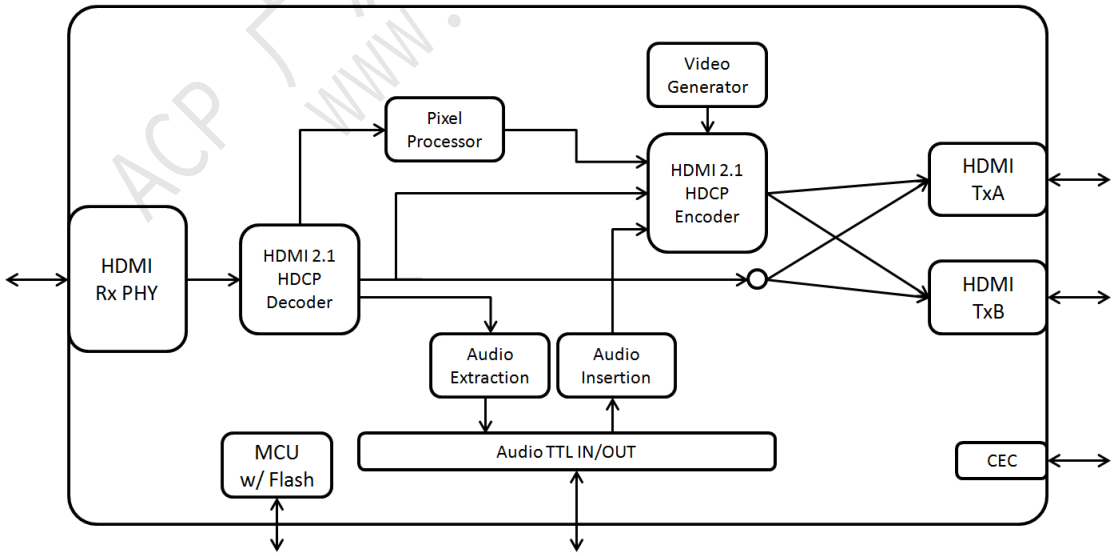

Figure 1. Top Diagram

The supported audio formats are listed in Table 1

Table 1. Supported Audio Format

Packet ID	Packet Type	Sampling Frequency (KHz)		
		32/44.1/48/88.2/ 96/176.4/192	256/352.8/384/ 512/705.6/768	64/128
0x02	Audio Sample Packet (LPCM and Compressed Audio)	Y		Y
0x07	One Bit Audio Sample Packet	Y		
0x08	DST Audio Packet	Y		
0x09	High Bit-rate Audio Stream Packet	Y	Y	

1.2 Features

1.2.1 HDMI Receiver

- Compliant with HDMI 2.1, HDMI 2.0b, HDMI 1.4b
- Compliant with HDCP 2.2/2.3 and HDCP 1.4 in repeater/receiver mode
- Data rate up to 48Gbps (FRL 12Gbps/4 Lane)
- Programmable Adaptive Equalization
- Support High Dynamic Range (HDR) and Dynamic/Static Metadata
- Support Variable Refresh Rate (VRR), FreeSync, G-Sync
- Support ALLM
- Support Forward Error Correction (FEC)
- Support DSC pass-through for compressed input timing
- Embedded arbitrary EDID (up to 512 bytes)
- 5V tolerance on DDC/HPD pins

1.2.2 HDMI Transmitter

- Compliant with HDMI 2.1, HDMI 2.0b, HDMI 1.4b
- Compliant with HDCP 2.2/2.3 and HDCP 1.4
- Data rate up to 48Gbps (FRL 12Gbps/4 Lane)
- Programmable Voltage Swing, Slew-Rate and Pre-emphasis
- Support AC-coupling on TMDS
- Support Color Space Converter in FRL and HDMI 2.0 mode
- Support HDR (HDR10/HDR10+/Dolby Vision/HLG)
- Support Variable Refresh Rate (VRR), FreeSync, G-Sync

- Support ALLM
- Support DSC encoded stream pass-through
- Hardware CEC Engine for Low Level protocol decoding
- 5V tolerance on DDC/HPD/CEC pins

1.2.3 Pixel Processor

- HDR to SDR conversion for HDR10, HDR10+, HLG and Low Latency DolbyVision
- Color Space conversion
- YCbCr 444-420 timing conversion
- Downscaler with selectable 2/3/4/8/16/32 ratio
- Deinterlacer for interlaced timing

1.2.4 Audio Input/Output

- I2S and SPDIF Audio Extraction from HDMI Rx
- I2S/SPDIF Audio Insertion to HDMI Tx
- SPDIF/I2S/HBR/DSD/TDM Format Supported for Audio Extraction and Insertion
- SPDIF to I2S Conversion using single TTL bus in Bi-direction

1.2.5 System Features

- Optional External MCU (via I2C)/ Internal MCU mode for chip control
- Embedded MCU and External Flash
- External pins of Flash QSPI interface
- External 25MHz Crystal required
- Available Pins for UART/Timer/GPIO
- Temperature Sensor Monitoring Circuit

1.3 Chip Application Modes

1.3.1 HDMI 1to2 Repeater with audio extraction

The default 1to2 repeater application mode of GSV6502 is that 2 HDMI outputs copy the same TMDS/FRL stream from HDMI input. Other than HDMI input lane frequency, GSV6502 HDMI Outputs have an advanced feature of generating a shared secondary FRL/TMDS lane frequency. For example, HDMI input timing is 4K@60Hz using FRL 12G/4Lane, and secondary lane frequency is set to HDMI 2.0 TMDS mode. Any of the 2 HDMI outputs can choose either default 4K@60Hz using FRL 12G/4Lane, or secondary 4K@60Hz using HDMI 2.0 TMDS mode.

Meanwhile, Audio extraction can be applicable if required.

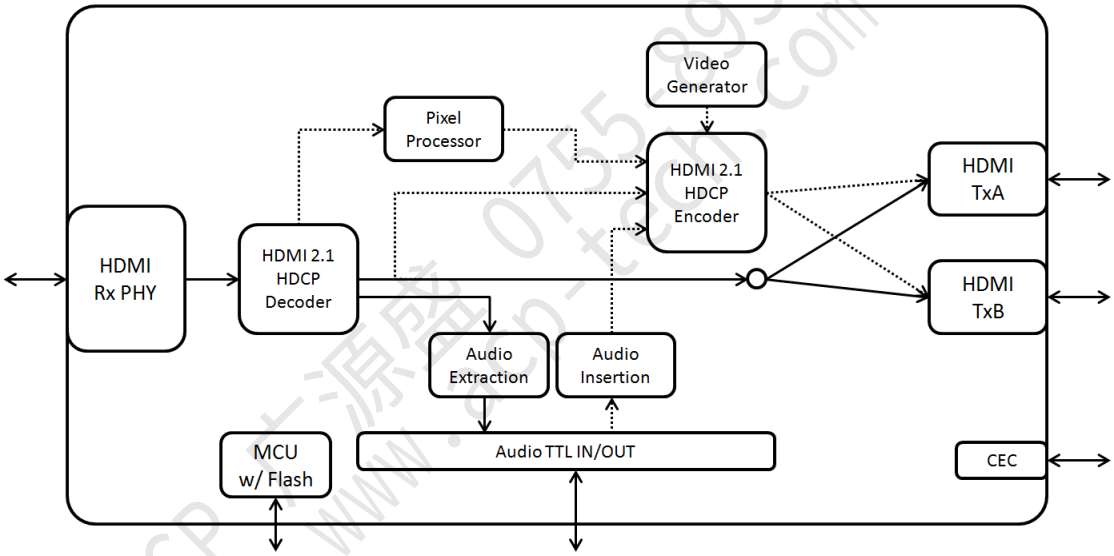

Figure 2. HDMI to HDMI 1to2 repeater with audio extraction

1.3.2 HDMI 1to2 Repeater with compatible HDMI 1.4 timing

Within bandwidth limitation, GSV6502 can keep input stream consistent and intact, while dynamically switch output between FRL and HDMI 2.0 mode for the best compatibility. For example, when FRL12G/4Lane 4K@60Hz timing is input, GSV6502 can convert to HDMI 2.0 or FRL 6G/3Lane, FRL 6G/4Lane, FRL 8G/4Lane, FRL 10G/4Lane, FRL 12G/4Lane as output. During HDMI output mode switch, HDMI input stream will not be disturbed.

GSV6502 can also support fixed output FRL rate, regardless of HDMI input mode. For

example, when HDMI 2.0 4K@30Hz is input, GSV6502 can convert it to FRL 10G/4Lane output. And when FRL 8G/4Lane 4K@120Hz is input, GSV6502 can still maintain FRL 10G/4Lane output with timing conversion.

And using pixel processor, For any HDMI 2.1 uncompressed timing, while most HDMI outputs can copy HDMI 2.1 input stream for HDMI 2.1 downstream devices. The secondary HDMI 1.4 or DVI timing with SDR color can be generated as output stream for any compatible HDMI 1.4 or DVI downstream devices.

Meanwhile, Audio extraction can be applicable if required.

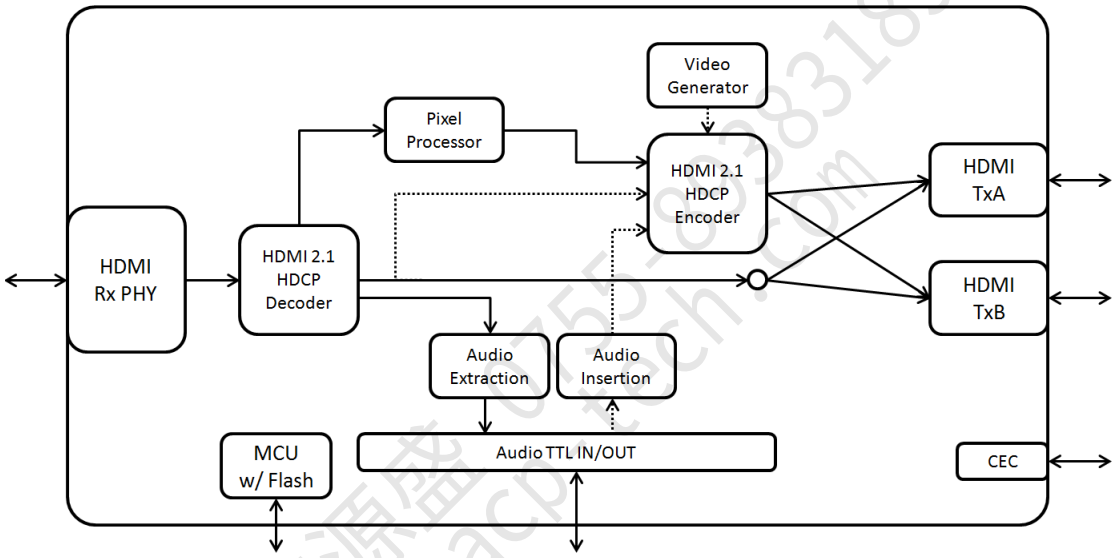

Figure 3. HDMI 1to2 repeater with compatible HDMI 1.4 timing

1.3.3 Audio Insertion for HDMI Tx

I2S/SPDIF audio stream and HDMI Rx video can be inserted into HDMI Tx. While video stream is the same, audio stream can be chosen between HDMI Rx audio or inserted audio.

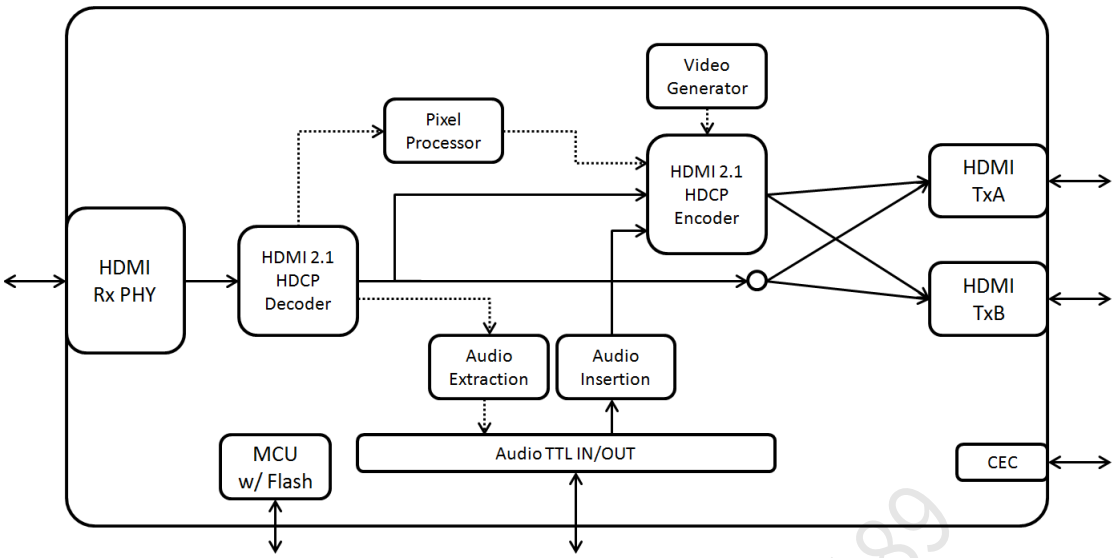

Figure 4. Audio Insertion Application

1.4 Audio Bus Output Configuration

When one group of audio bus is configured as output, I2S and SPDIF are output at the same time. General configuration of pin settings is shown below:

Table 2. I2S/SPDIF Audio Extraction

Pin Name	Alias	Direction	Description
AUD_D0	SDATA[0]	Output	I2S Data, default stereo channels
AUD_D5	LRCLK/WS	Output	Fs (0 = Left, 1 = Right)
SCLK	BCLK	Output	Fixed to 64Fs
MCLK	Sys Clock	Output	Selected from 128Fs/256Fs/384Fs/512Fs

For HBR application, it is also capable of sending out SPDIF in 4-pin mode.

Table 3. HBR Audio Extraction in SPDIF

Pin Name	Alias	Direction	Description
AUD_D0	SPDIF[0]	Output	SPDIF Data[0], 1/2 channels

1.5 Audio Bus Input Configuration

When Audio Bus is set to Input, either I2S or SPDIF can be selected. It should be noted that external MCLK is required in I2S audio insertion mode.

For SPDIF input, GSV6502 can detect Sampling Frequency and automatically update it into Channel Status with GSV software. For I2S input, software designer needs to indicate the input sampling frequency in software.

General application modes are listed below.

Table 4. Stereo I2S Input

Pin Name	Alias	Direction	Description
AUD_D0	SDATA[0]	Input	I2S Data, default stereo channels
AUD_D5	LRCLK/WS	Input	Fs (0 = Left, 1 = Right)
SCLK	BCLK	Input	Fixed to 64Fs
MCLK	Sys Clock	Input	Selected from 128Fs/256Fs/384Fs/512Fs

Table 5. SPDIF Input

Pin Name	Alias	Direction	Description
AUD_D0	SPDIF	Input	SPDIF channel

Table 6. 8-Channel I2S Input

Pin Name	Alias	Direction	Description
AUD_D0	SDATA[0]	Input	I2S Data, default stereo channels
AUD_D5	LRCLK/WS	Input	Fs (0 = Left, 1 = Right)
SCLK	BCLK	Input	Fixed to 64Fs
MCLK	Sys Clock	Input	Selected from 128Fs/256Fs/384Fs/512Fs

1.6 Audio Bus Input/Output Bi-Direction Configuration

When bi-direction is needed for a single audio bus, stereo audio insertion and extraction can be simultaneously supported.

Table 7. I2S Audio Insertion and Extraction in Bi-Direction

Pin Name	Alias	Direction	Description
AUD_D0	SDATA[0]	Output	I2S Data, default stereo channels
AUD_D5	LRCLK/WS	Input	Fs (0 = Left, 1 = Right)
SCLK	BCLK	Input	Fixed to 64Fs
MCLK	Sys Clock	Input	Selected from 128Fs/256Fs/384Fs/512Fs